IN THE CLAIMS

Cancel Claims 1 and 2. Re-write Claim 3 as follows. Add new Claims 13-23.

1. (canceled)

2. (canceled)

3. (currently amended) A method of fabricating a one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cell, the method comprising:

forming a buried region having a first conductivity type below an upper surface of a semiconductor region of a semiconductor substrate, the semiconductor region having a second conductivity type, opposite the first conductivity type; and

forming a field-effect transistor in the semiconductor region over the buried region, the field effect transistor having a source and a drain, wherein the buried region, the source and the drain are formed such that a depletion region is located between the buried region, ~~and~~ the source~~,~~ and the drain ~~and body regions of the field-effect transistor~~, the depletion region defining a floating body region of the field effect transistor, and providing the sole lateral isolation for portions of the floating body region.

4. (original) The method of Claim 3, wherein the buried region is formed by an ion implantation step.

5. (original) The method of Claim 4, wherein the buried region is implanted through a first mask.

6. (original) The method of Claim 5, further comprising performing a threshold voltage adjustment implant having the second conductivity type through the first mask.

7. (original) The method of Claim 3, further comprising forming one or more shallow trench isolation regions that extend a first depth into the semiconductor substrate.

8. (original) The method of Claim 7, further comprising implanting the buried region such that the buried region has a top interface located at or above the first depth in the semiconductor substrate, and a bottom interface located below the first depth in the semiconductor substrate.

9. (original) The method of Claim 3, wherein the field-effect transistor is fabricated using a process compatible with a standard CMOS process.

10. (original) The method of Claim 3, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the buried region contacts the well region.

11. (original) The method of Claim 3, further comprising forming a deep well region having the first conductivity type in the semiconductor substrate, wherein the deep well region is located below and continuous with the buried region.

12. (original) The method of Claim 11, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the well region contacts the deep well region.

13. (New) A method of fabricating a plurality of one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cells, the method comprising:

forming a buried region having a first conductivity type below an upper surface of a semiconductor region of a semiconductor substrate, the semiconductor region having a second conductivity type, opposite the first conductivity type; and

forming a plurality of rows of field-effect transistors in the semiconductor region over the buried region, each of the field effect transistors having a source and a drain, wherein the buried region, and each source and drain are formed such that a continuous depletion region is located between the buried region and each source and drain, the depletion region defining floating body regions of the field effect transistors, and providing lateral isolation for floating body regions located in adjacent rows.

14. (New) The method of Claim 13, wherein the step of forming a plurality of rows of field-effect transistors comprises forming a plurality of word lines, wherein each of the word lines is associated with a corresponding row of the field effect transistors.

15. (New) The method of Claim 13, wherein the buried region is formed by an ion implantation step.

16. (New) The method of Claim 15, wherein the buried region is implanted through a first mask.

17. (New) The method of Claim 16, further comprising performing a threshold voltage adjustment implant having the second conductivity type through the first mask.

18. (New) The method of Claim 13, further comprising forming one or more shallow trench isolation regions that extend a first depth into the semiconductor substrate, wherein the shallow trench isolation regions provide lateral isolation for field effect transistors located in the same row.

19. (New) The method of Claim 18, further comprising implanting the buried region such that the buried region has a top interface located at or above the first depth in the semiconductor substrate, and a bottom interface located below the first depth in the semiconductor substrate.

20. (New) The method of Claim 13, wherein the field-effect transistors are fabricated using a process compatible with a standard CMOS process.

21. (New) The method of Claim 13, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the buried region contacts the well region.

22. (New) The method of Claim 13, further comprising forming a deep well region having the first conductivity type in the semiconductor substrate, wherein the deep well region is located below and continuous with the buried region.

23. (New) The method of Claim 22, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the well region contacts the deep well region.